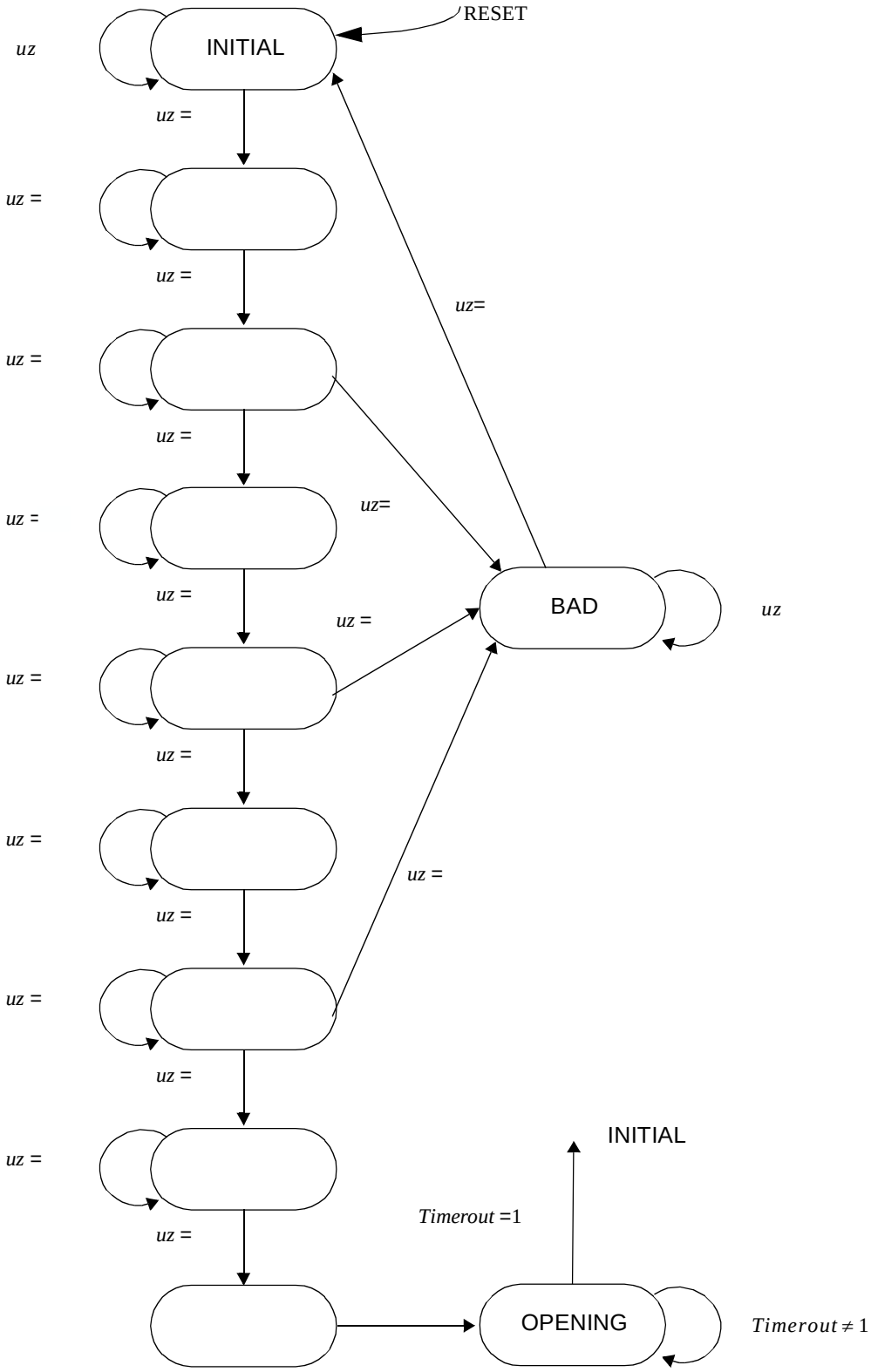
Name: _____ **Student ID:** _____

On page 2 of our number lock lab, we have provided a completed 11-state state diagram for a secret number code of 1011.

Please complete the following blank 11-state state diagram for a different secreat code 0100 (just the opposite of 1011).

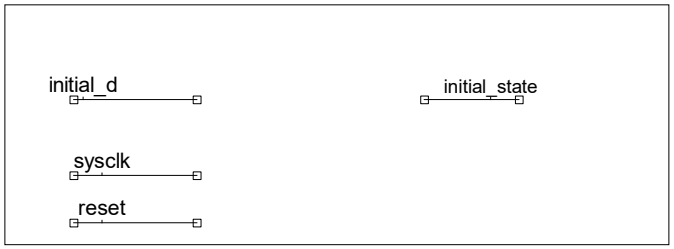
QP1
Page total: 15

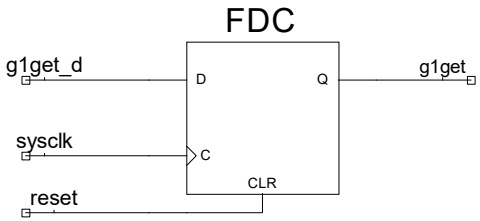
For a secret code of 0100

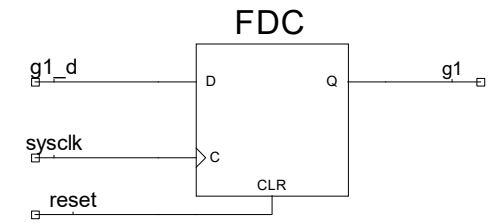


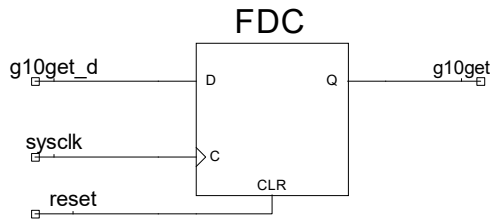
State Machine for the Number Lock

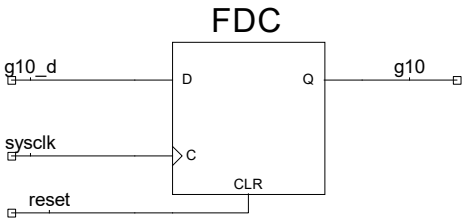
QP2 Page total: 15

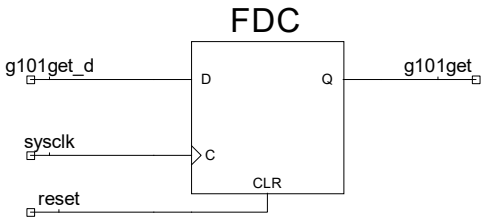


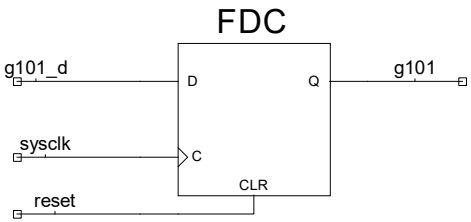


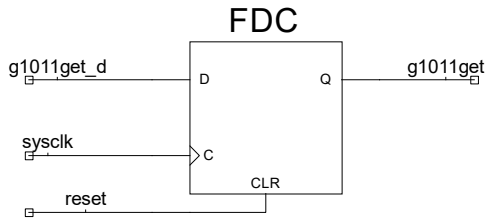


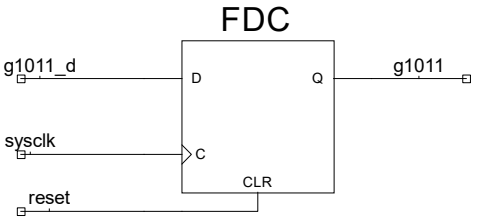


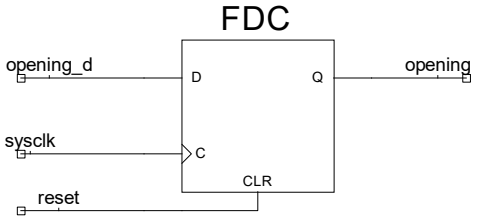


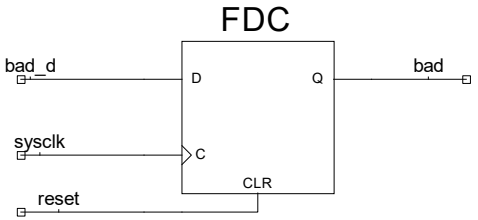


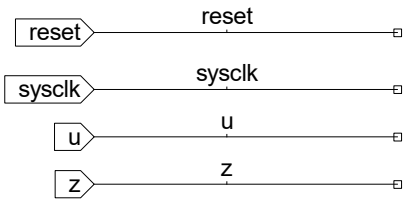


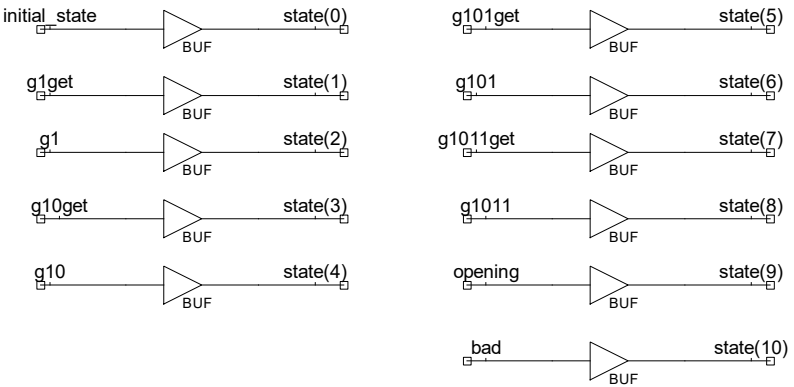












USC VSoE CENG
EE201L Lab

Experiment:	Sheet
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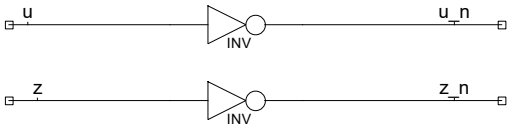
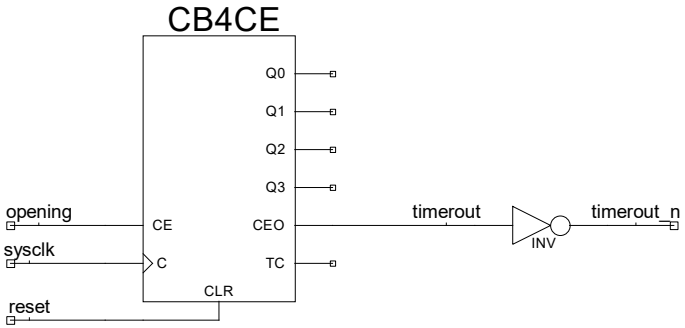
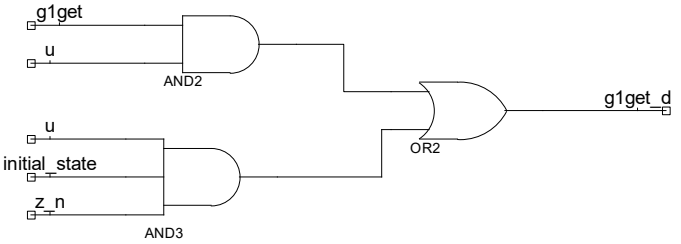
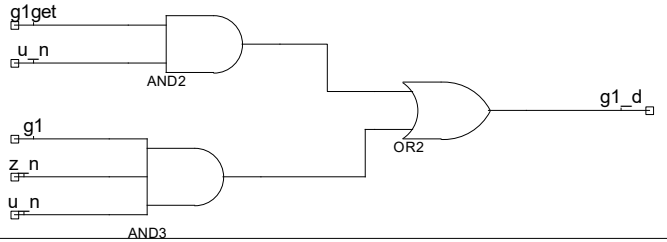
Student: Date	

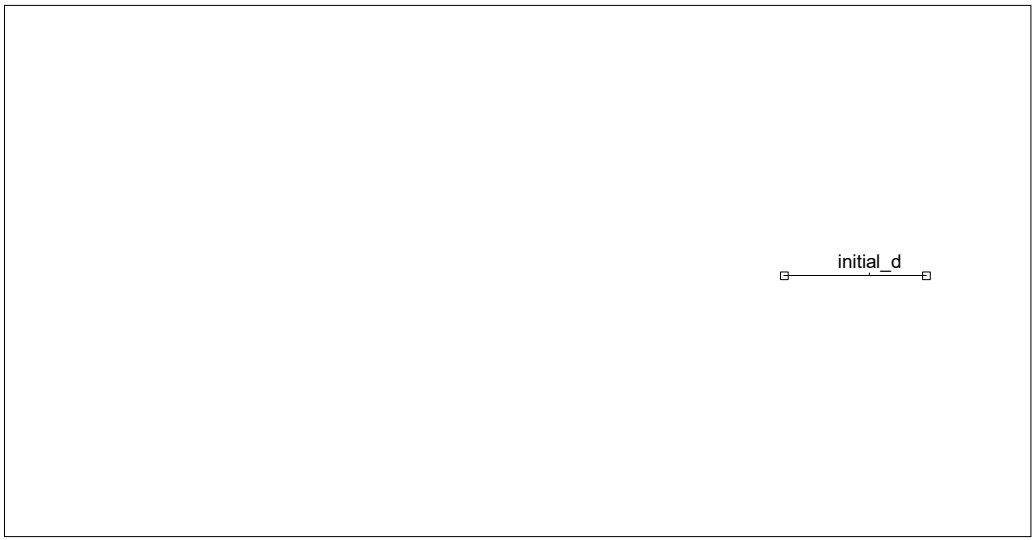
QP3 Page total: 15

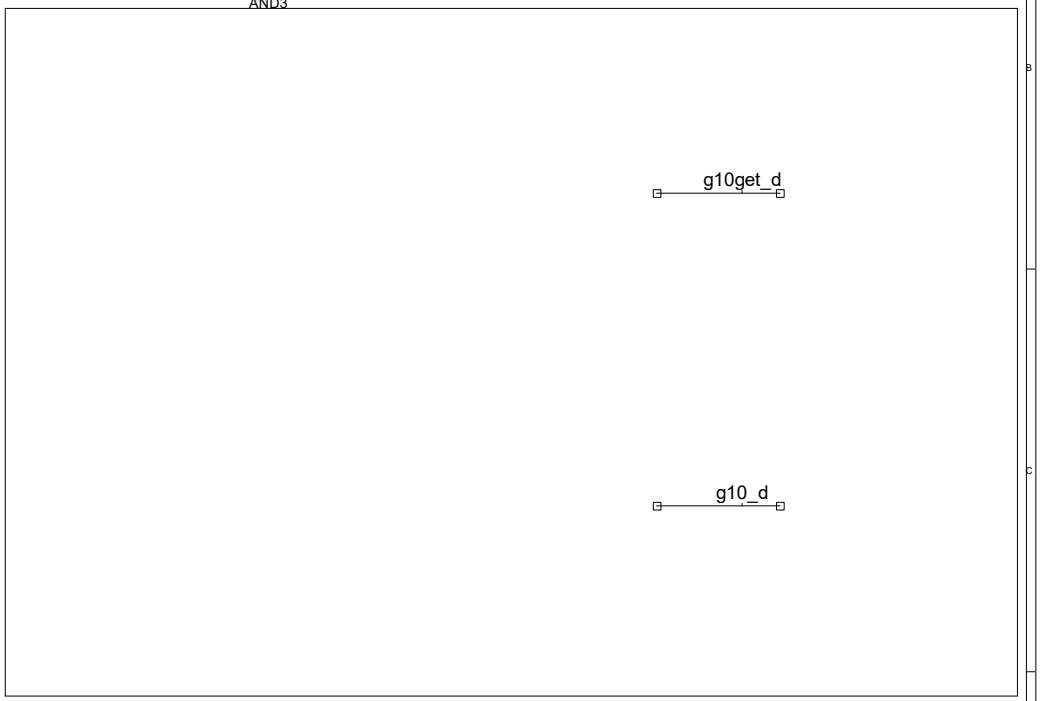


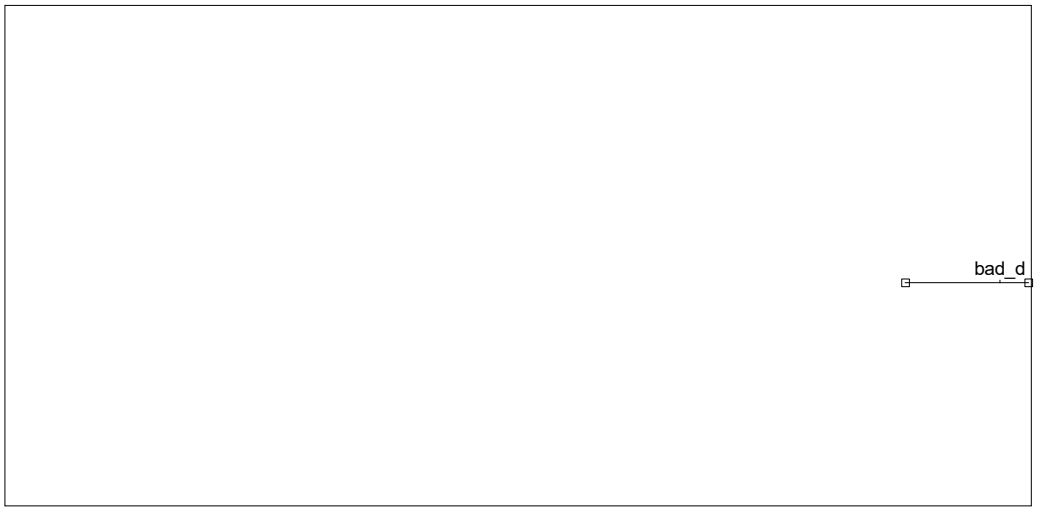


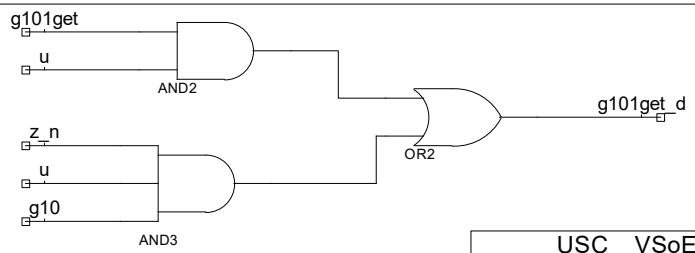












USC VSoE CENG	
EE201L Lab	
Experiment:	Sheet
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Student: Date	

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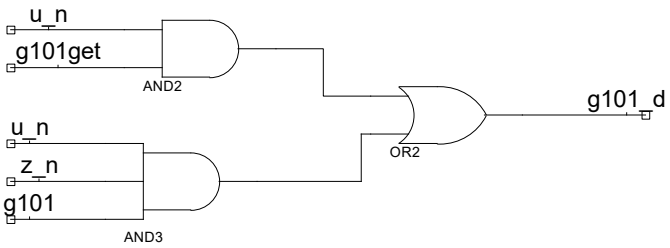

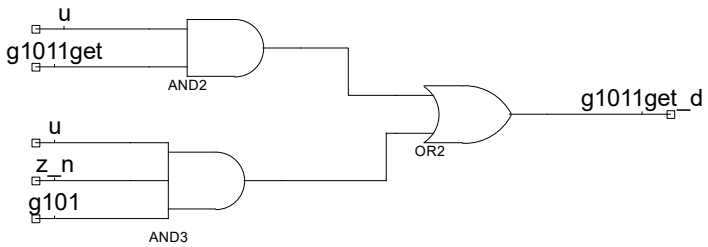

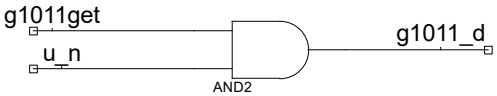

USC VSoE CENG	
EE201L Lab	
Experiment:	Sheet
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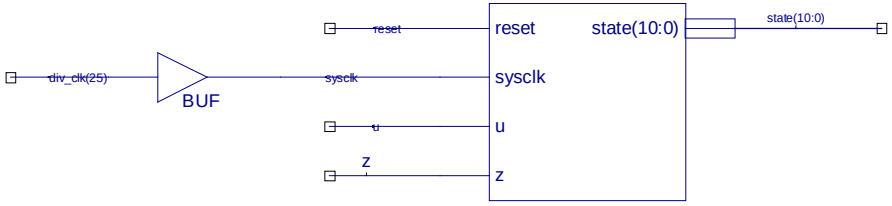
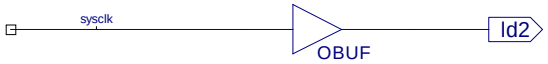
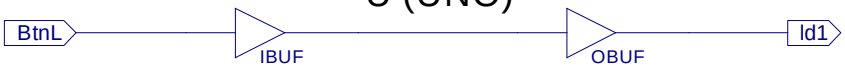
Student: Date	

ee201l_number_lock



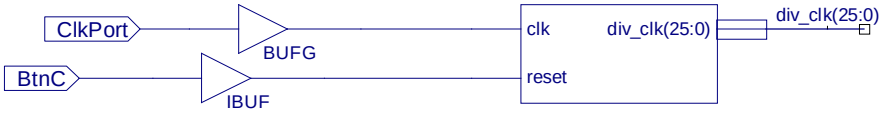


U (UNO)

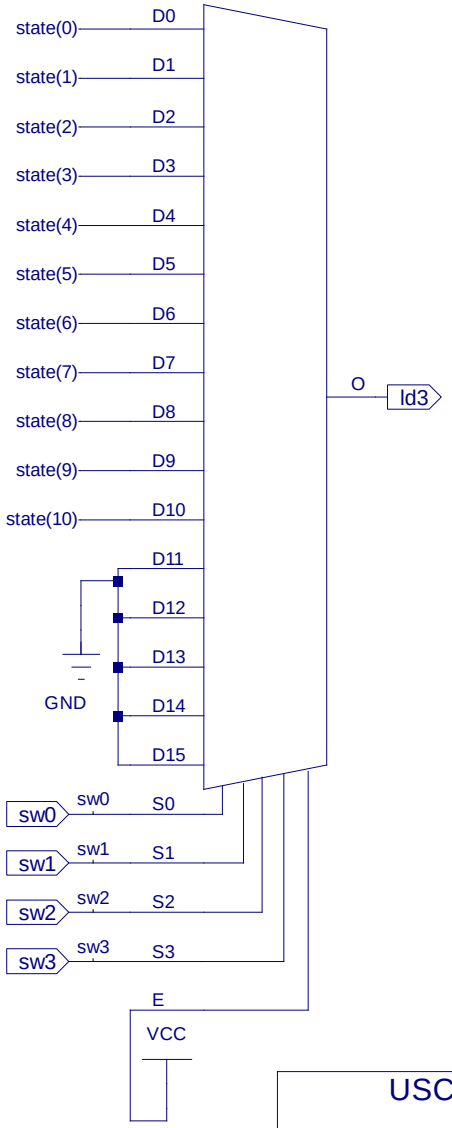


Z (ZERO)

clock_divider



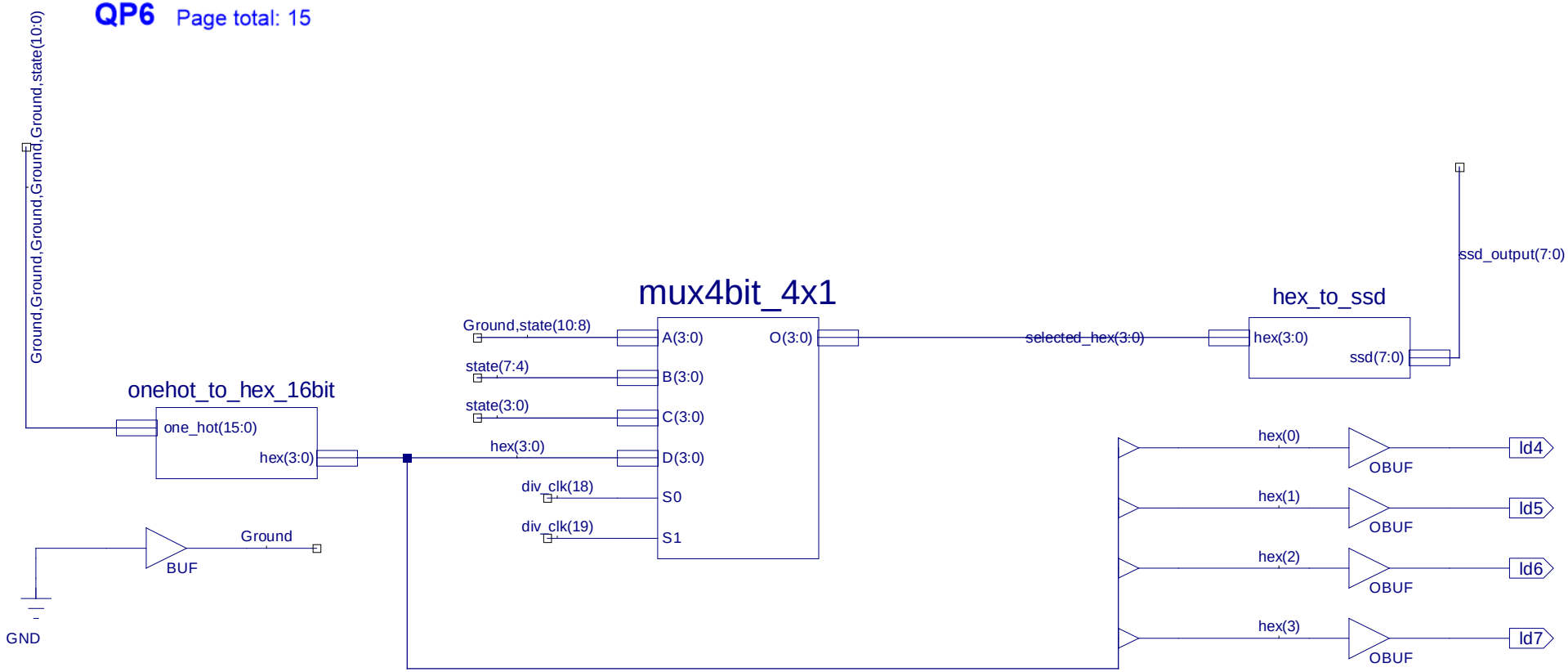
M16_1E

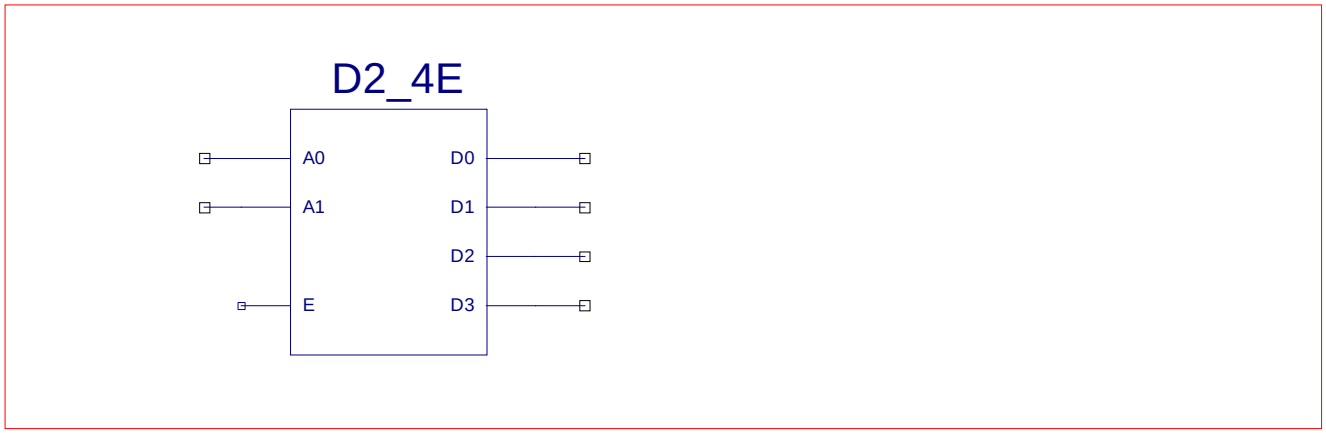


Sheet 1/3 Already complete!

USC VSoE CENG	
EE201L Lab	
Experiment: Number Lock Top	Sheet 1/3
Designed by: Gandhi Puvvada Date	Drawn by: Date
Student: Date	

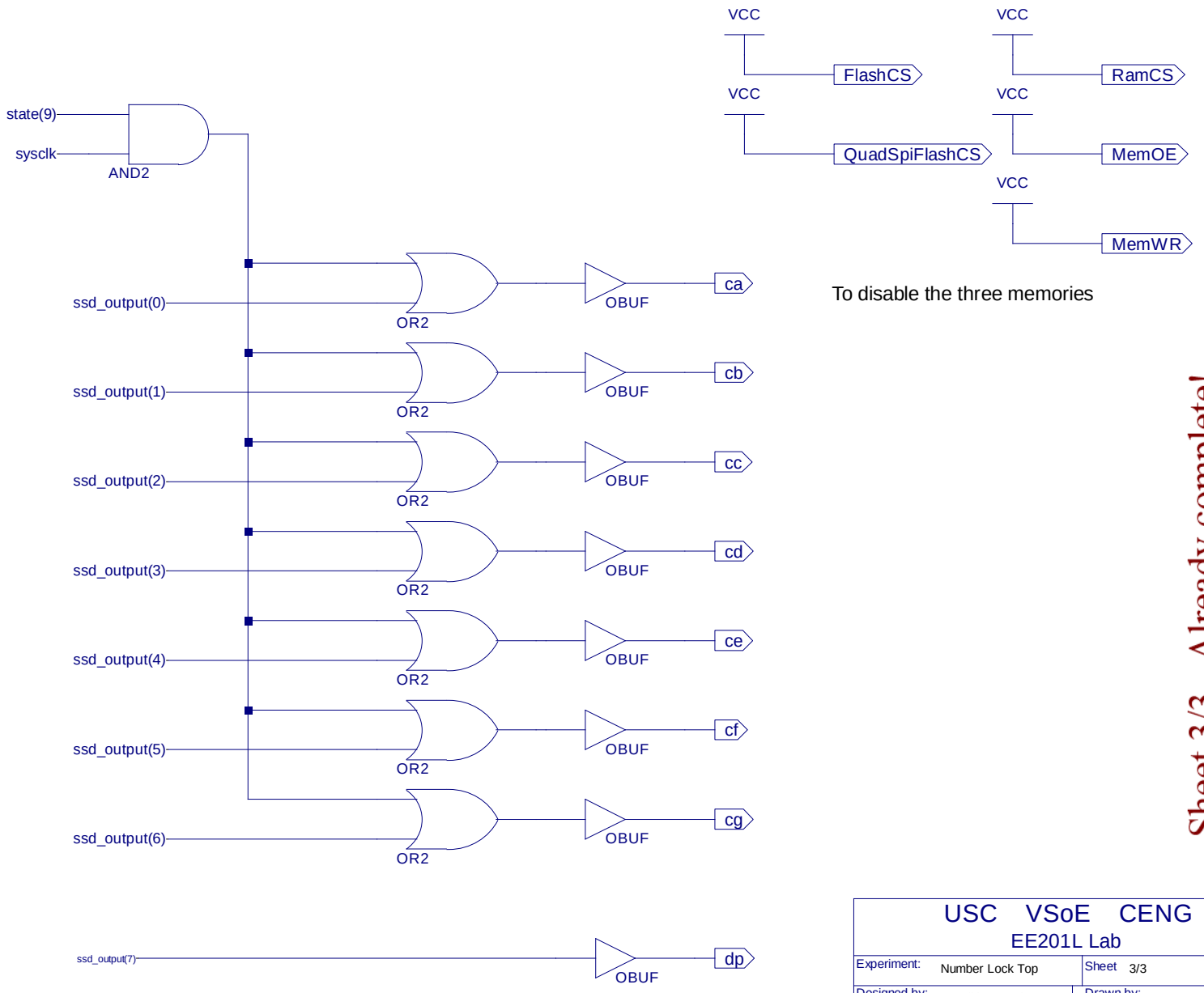
QP6 Page total: 15





Sheet 2/3 To be completed by students

USC VSoE CENG EE201L Lab	
Experiment: Number Lock Top	Sheet 2/3
Designed by: Gandhi Puvvada Date	Drawn by: Date
Student: Date	



To disable the three memories

Sheet 3/3 Already complete!

USC VSoE CENG	
EE201L Lab	
Experiment: Number Lock Top	Sheet 3/3
Designed by: Gandhi Puvvada Date	Drawn by: Date
Student: Date	

4. Lab Report:

Name:_____	Date: _____
Lab Session:_____	TA's Signature: _____

For TAs: Paper design, Simulation of a compiled core, and analysis, synthesis and generation of .bit file, and demo (70 points): _____ Report (30 points): _____
Comments:

Q 4. 1: You have simulated the core design, **`ee201_numlock_sm.v`** using **`ee201_numlock_sm_tb.v.`** Attach (to the report) the simulation waveform for a/the test case which led you open the lock.

Q 4. 2: Complete the following three items and attach them to this report.
`Number_Lock_state_digram_exercise_for_0100_code.pdf`
`ee201l_number_lock_core_3page_schematic.pdf`
`ee201l_number_lock_top_3page_schematic.pdf`

Q 4. 3: What is the reason for commenting out the **`BtnU`** and **`BtnD`** lines in the .xdc file (**`ee354_top.xdc)`**(2 pts)?

```
#Bank = 15, Pin name = IO_L14P_T2_SRCC_15,    Sch name = BTNU
#set_property PACKAGE_PIN F15 [get_ports BtnU]
#set_property IOSTANDARD LVCMOS33 [get_ports BtnU]

#Bank = 14, Pin name = IO_L21P_T3_DQS_14,     Sch name = BTND
#set_property PACKAGE_PIN V10 [get_ports BtnD]
#set_property IOSTANDARD LVCMOS33 [get_ports BtnD]
```

Q 4. 4: Fill-up the frequencies of the clock divider (6 pts)

Q 4. 5: Flashing effect created in the OPENING state: Refer to section 3.12 above. Suppose we replace the seven 2-input OR gates with seven 2-input NAND gates . What other modifications you need to make to your circuit in order to make it work? Think about DeMorgan's theorem! (6 pts)

Assume that the input clock (ClkPort) frequency is '
Frequency of div_clk[21] = $f/2^X$ where X =____
Frequency of div_clk[23] = $f/2^Y$ where Y =____
Frequency of div_clk[13] = $f/2^Z$ where Z =____
Frequency of div_clk[1] = $f/2^P$ where P =____
Frequency of div_clk[2] = $f/2^Q$ where Q =____
Frequency of div_clk[24] = Frequency of sysclk =
= $f/2^R$ where R =____

Q 4. 6: Refer to section 3.11: What would you do to change the display of nine to  from  (6 pts)

HexDigit	hex(3)	hex(2)	hex(1)	hex(0)	Cg	Cf	Ce	Cd	Cc	Cb	Ca	dp
0	0	0	0	0	1	0	0	0	0	0	0	1
1	0	0	0	1	1	1	1	1	0	0	1	1
2	0	0	1	0	0	1	0	0	1	0	0	1
3	0	0	1	1	0	1	1	0	0	0	0	1
4	0	1	0	0	0	0	1	1	0	0	1	1
5	0	1	0	1	0	0	1	0	0	1	0	1
6	0	1	1	0	0	0	0	0	0	1	0	1
7	0	1	1	1	1	1	1	1	0	0	0	1
8	1	0	0	0	0	0	0	0	0	0	0	1
9	1	0	0	1	0	0	1	0	0	0	0	1
A	1	0	1	0	0	0	0	1	0	0	0	1
b	1	0	1	1	0	0	0	0	0	1	1	1
C	1	1	0	0	1	0	0	0	1	1	0	1
d	1	1	0	1	0	1	0	0	0	0	1	1
E	1	1	1	0	0	0	0	0	1	1	0	1
F	1	1	1	1	0	0	0	1	1	1	0	1
ROM (Look Up Table) Values ========>					1083	208E	02BA	8492	D004	D860	2812	FFFF

Q 4. 7: Suppose that you could press a button **exactly** for one clock period. State why the following state diagram does not work. Fix the state diagram. Include a "**BAD**" state. (10 pts)