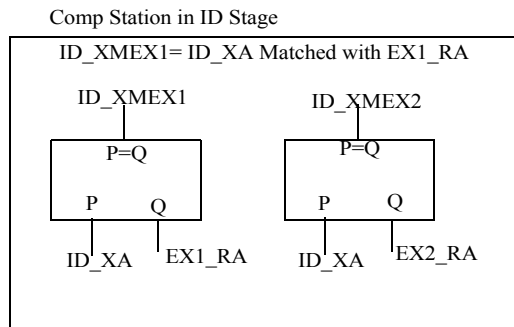
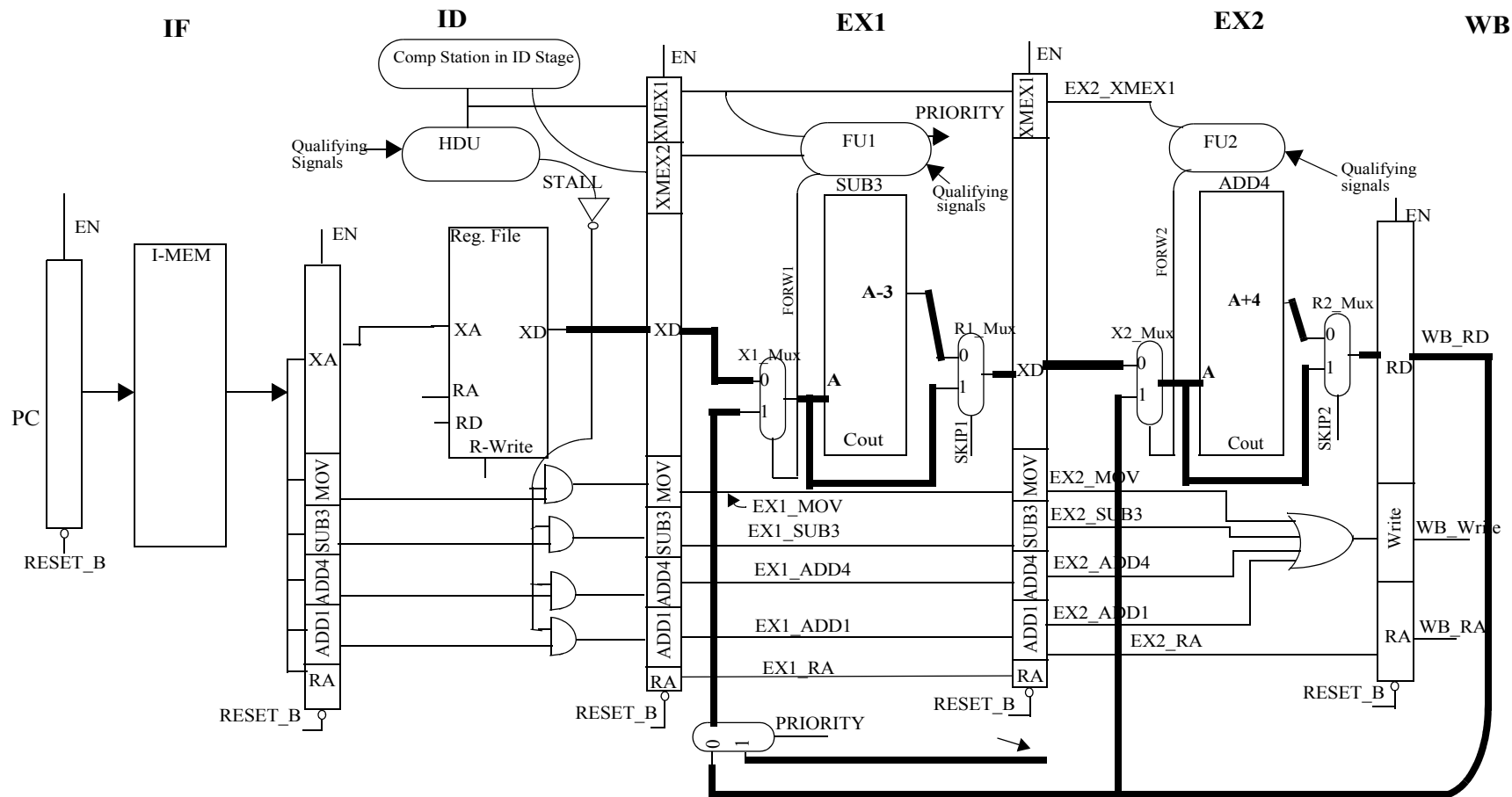




1. Complete all missing connections to the Reg. File.
Also complete the RA(Result Addreee) connection in ID stage (ID_RA).
2. Complete all five enable (EN) controls on the pipeline registers (including PC).
3. Complete the forwarding path from EX2 to EX1. Should it start from upstream or downstream of the X2_mux?
4. Complete the skip controls(SKIP1,SKIP2).
5. Draw the logic for the HDU, FU1, and FU2, producing STALL, PRIORITY, FORW1, FORW2.

LAB 7 Part 3 Block Diagram

Fig. 1