ICM7218 Series CMOS Universal 8 Digit LED Driver System

FEATURES

- **Total circuit integration on chip includes:**
  - **a) Digit and segment drivers**
  - **b) All multiplex scan circuitry**
  - **c) 8X8 static memory**
  - **d) 7 segment Hexadecimal and Code B decoders**
- **Output drive suitable for large LED displays**
- **Both common anode and common cathode LED drive versions**
- **Single 5 volt supply required**
- **Data retention to 2 volts supply**
- **Shutdown feature - turns off display and puts chip into very low power dissipation mode**
- **Pin selectable choice of 2 seven segment decoders - Hexa or Code B**
- **Pin selectable choice of seven segment decode or no decoder**
- **Microprocessor compatible and hardwire versions**
- **All terminals protected against static discharge**

GENERAL DESCRIPTION

The ICM7218 series of universal LED driver systems provide, in a single package, all the circuitry necessary to interface most common microprocessors or digital systems and an LED display. Included on chip is an 8x8 static memory array providing storage for the displayed information, 2 types of 7 segment decoders, all the multiplex scan circuitry and the high power digit and segment drivers.

The ICM7218A and ICM7218B are intended to be used primarily in microprocessor systems. Data is read directly from the I/O bus line from the microprocessor. 2 Control lines ($\overline{\text{Write}}$, and Mode) define chip select, which reads either 4 bits of control information (Data Coming, $\overline{\text{Shutdown}}$, Decode, Hexa or Code B Decoding) or 8 bits of Display Input Data. Display Input Data (8 words, 8 bits each) is automatically sequenced into the memory on successive negative going $\overline{\text{Write}}$ pulses. Data may be displayed either directly or decoded in Hexadecimal or Code B formats. The ICM7218A drives a common anode display while the ICM7218B drives a common cathode display. (See Block Diagram 1)

The ICM7218C and ICM7218D feature 2 lines for control information ($\overline{\text{Write}}$, Three Level Input; Hexa, Code B, $\overline{\text{Shutdown}}$), 4 lines for Input Data and 3 lines for BCD Data Addressing of each of eight data memory locations.

Data is written into memory by setting up a BCD Data Address memory location, defining 4 lines of Input Data and then strobe the $\overline{\text{Write}}$ line low. The Three Level Control Input is independent of the $\overline{\text{Write}}$ instruction. Only Hexadecimal and Code B decoding are available for the Display Outputs. The ICM7218C drives a common anode display, the ICM7218D a common cathode display. (See Block Diagram 2)

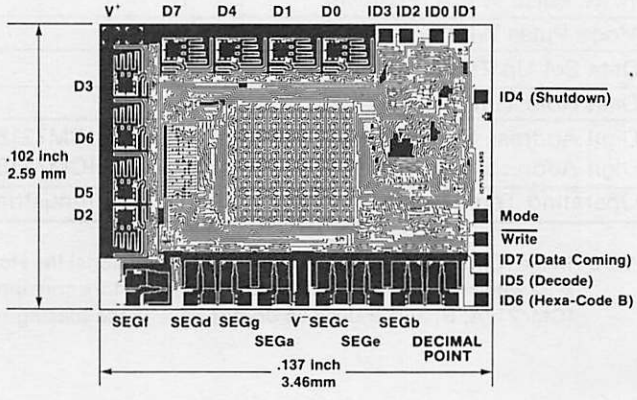
The ICM7218E provides 4 separate lines for control information ($\overline{\text{Write}}$, Hexa-Code B, Decode, $\overline{\text{Shutdown}}$), 8 lines for input data, and 3 lines for BCD digit address. Data is written into the memory by setting up a BCD Data Address memory location, defining 8 lines of Input Data, and then strobe the $\overline{\text{Write}}$ line low. Control information is on separate lines and is independent of the $\overline{\text{Write}}$ instruction. Data may be displayed either directly or decoded in Hexadecimal or Code B formats. The ICM7218E drives a common anode display. (See Block Diagram 3)

ORDERING INFORMATION

Typical App.	Order Part Number	Display Option	Package
Microprocessor Control	ICM7218A IJI	Common Anode	28 Lead CERDIP
	ICM7218B IPI	Common Cathode	28 Lead Plastic
Hardwire Control	ICM7218C IJI	Common Anode	28 Lead CERDIP
	ICM7218D IPI	Common Cathode	28 Lead Plastic
	ICM7218E IDL	Common Anode	40 Lead Ceramic

This is a preliminary specification and is subject to change.

CHIP TOPOGRAPHY ICM7218A



INTERSIL, INC., 10710 N. TANTAU AVE., CUPERTINO, CA 95014 (408) 996-5000 TWX: 910-338-0171

Printed in U.S.A.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	6V
Digit Output Current	300mA
Segment Output Current	50mA
Input Voltage (any terminal)	$V^+ + 0.3V$ to $V^- - 0.3V$ NOTE 1
Power Dissipation (28 Pin CERDIP)	1 watt NOTE 2
Power Dissipation (28 Pin Plastic)	0.5 watt NOTE 2
Power Dissipation (40 Pin Ceramic)	1 watt NOTE 2
Operating Temperature Range	−20°C to +70°C
Storage Temperature Range	−55°C to +125°C

NOTE 1 Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V^+ or less than V^- may cause destructive device latchup. For this reason it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established. When using multiple supply systems the supply to the ICM7218 should be turned on first.

NOTE 2 These limits refer to the package and will not be obtained during normal operation. Derate above 50°C by 25mW per °C.

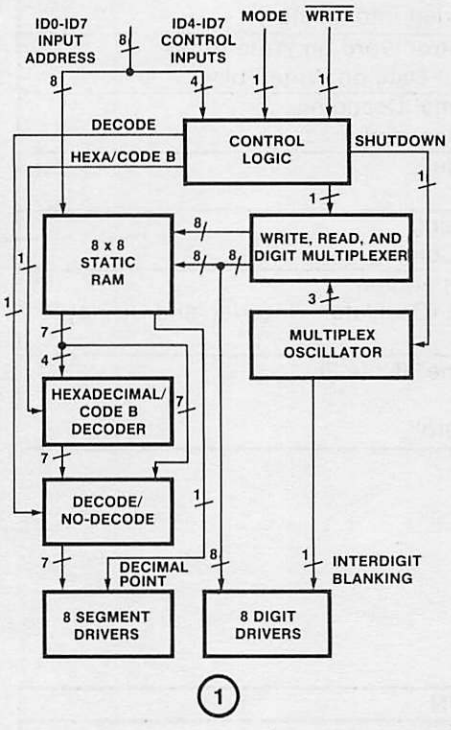
SYSTEM ELECTRICAL CHARACTERISTICS V^+-V^- = 5V, T_A = 25°C, Test Circuit, Display Diode Drop 1.7V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage	V^+-V^-		4		6	V
	V^+-V^-	Power Down Mode	2		6	V
Quiescent Supply Current	I_Q	Shutdown (Note 3)	6	10	300	μA
Operating Supply Current	I_{DP}	Decoder On, Outputs Open Ckt	250		950	μA
		No Decode, Outputs Open Ckt	200		450	μA
Digit Drive Current	I_D	Common Anode Vout = $V^+ - 2.0$	−170			mA
		Common Cathode Vout = $V^- + 1V$	50			mA
Digit Leakage Current	I_{DL}				100	μA
Peak Segment Drive Current	I_S	Common Anode Vout = $V^- + 1.5V$	20			mA
		Common Cathode Vout = $V^+ - 2.0V$	−10			mA
Segment Leakage Current	I_{SL}				50	μA
Display Scan Rate	F_{MUX}			250		Hz
Three Level Input						
Logical "1" Input Voltage	V_{TH}	Hexidecimal ICM7218C, D (Pin 9)	4.0			V
Floating Input	V_{TD}	Code B ICM7218C, D (Pin 9)	2.0		3.0	V
Logical "0" Input Voltage	V_{TL}	Shutdown ICM7218C, D (Pin 9)			1.75	V
Three Level Input Impedance				100		kΩ
Logical "1" Input Voltage	V_{IH}		2.4			V
Logical "0" Input Voltage	V_{IL}				.8	V
Write Pulse Width (Negative)	tw		400			nS
Write Pulse Width (Positive)	$t\overline{w}$		400			nS
Mode Pulse Width	tm		400			nS
Data Set Up Time	t_{ds}		400			nS
Data Hold Time	t_{dh}		25			nS
Digit Address Set Up Time	t_{das}	ICM7218	400			nS
Digit Address Hold Time	t_{dah}	ICM7218	100			nS
Operating Temperature Range	T_A	Industrial Temperature Range	−20		70	°C

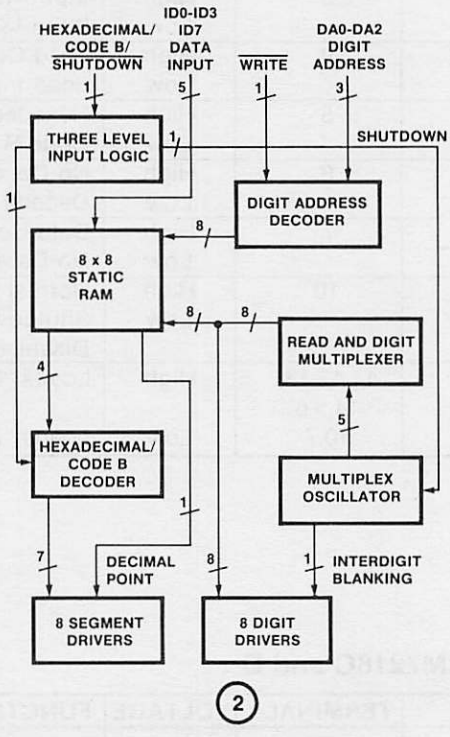
NOTE 3 In the ICM7218C and D (hardwire control versions) the Hexa/Code B/$\overline{\text{Shutdown}}$ Input (Pin 9) has internal biasing resistors to hold it at $V^+/2$ when Pin 9 is open circuited. These resistors consume power and result in a Quiescent Supply Current (I_Q) of typically 50μA. The ICM7218A, B, and E devices do not have these biasing resistors and thus are not subject to this condition.

BLOCK DIAGRAMS

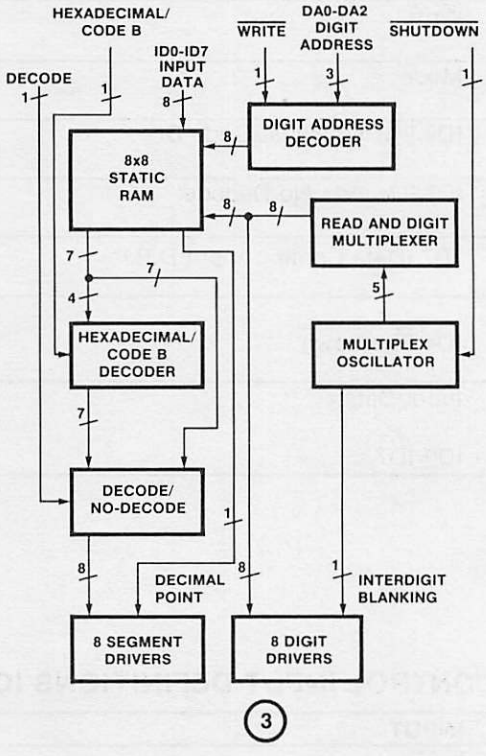
ICM7218A, ICM7218B



ICM7218C, ICM7218D



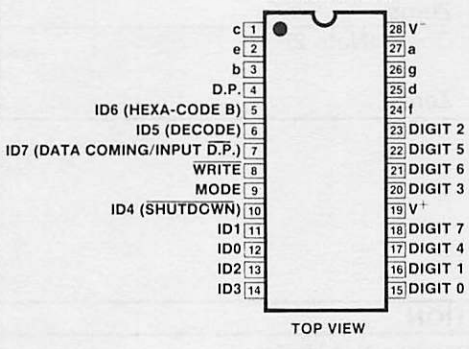
ICM7218E



PIN CONFIGURATION

ICM7218A

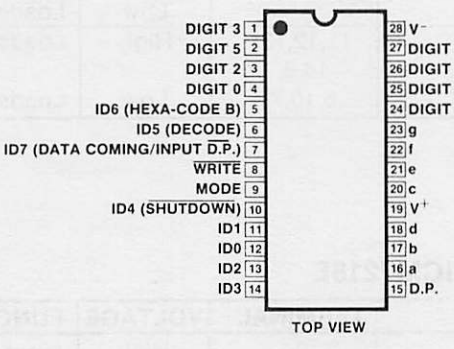
COMMON ANODE



TOP VIEW

ICM7218B

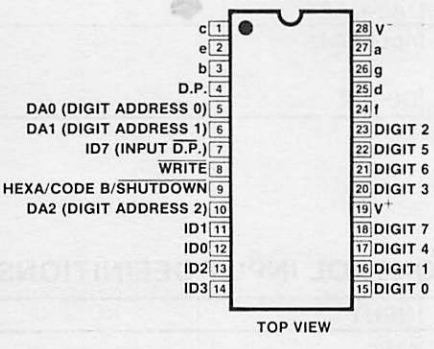
COMMON CATHODE



TOP VIEW

ICM7218C

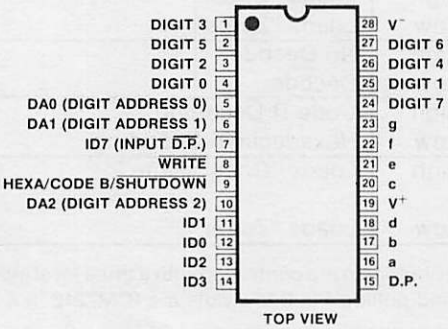
COMMON ANODE



TOP VIEW

ICM7218D

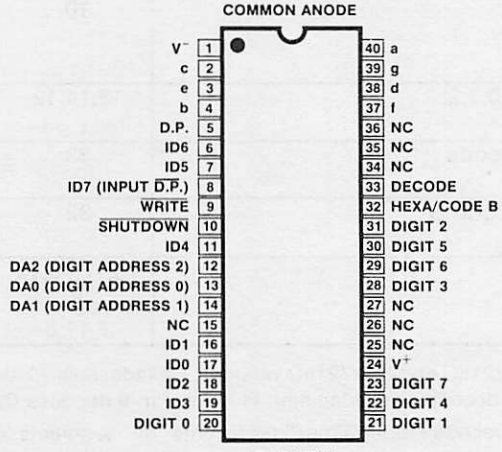
COMMON CATHODE



TOP VIEW

ICM7218E

COMMON ANODE



TOP VIEW

CONTROL INPUT DEFINITIONS ICM7218A and B

INPUT	TERMINAL	VOLTAGE	FUNCTION
$\overline{\text{Write}}$	8	High Low	Input Not Loaded Into Memory Input Loaded Into Memory
Mode	9	High Low	Load Control Word on Write Pulse Load Input Data on Write Pulse
ID6 (Hexadecimal/Code B)	5	High Low	Hexadecimal Decoding Code B Decoding
ID5 (Decode/No Decode)	6	High Low	No Decode Decode
ID7 (Data Coming/Input $\overline{\text{D.P.}}$)	7	High Low	Data Coming No Data Coming
ID4 $\overline{\text{Shutdown}}$	10	High Low	Normal Operation Shutdown (Oscillator, Decoder, and Displays Disabled)
Input Data ID0-ID7	11,12,13, 14,5,6 10,7	High Low	Loads "One" (Note 2) Loads "Zero"

CONTROL INPUT DEFINITIONS ICM7218C and D

INPUT	TERMINAL	VOLTAGE	FUNCTION
$\overline{\text{Write}}$	8	High Low	Inputs Not Loaded Into Memory Inputs Loaded Into Memory
Three Level Input (Note 1)	9	High Floating Low	Hexadecimal Decode Code B Decode Shutdown (Oscillator, Decoder and Displays Disabled)
Digit Address DA0-DA2	5,6,10	High Low	Loads "Ones" Loads "Zeros"
Input Data ID0-ID7	11,12,13, 14,5, 6,10,7	High Low	Loads "Ones" (Note 2) Loads "Zeros"

CONTROL INPUT DEFINITIONS ICM7218E

INPUT	TERMINAL	VOLTAGE	FUNCTION
$\overline{\text{Write}}$	9	High Low	Input Latches Not Updated Input Latches Updated
$\overline{\text{Shutdown}}$	10	High Low	Normal Operation Shutdown (Oscillator, Decoder and Displays Disabled)
Digit Address (0,1,2) DA0-DA2	13,14,12	High Low	Loads "Ones" Loads "Zeros"
Decode/No Decode	33	High Low	No Decode Decode
Hexadecimal/Code B	32	High Low	Code B Decoding Hexadecimal Decoding
Input Data ID0-ID7	16,17,18,19 6 7,11,8	High Low	Loads "Ones" (Note 2) Loads "Zeros"

NOTE 1 In the ICM7218C and ICM7218D versions, Hexadecimal, Code B and Shutdown are controlled with a three level input on Pin 9. Pulling Pin 9 high decodes Hexadecimal. Floating Pin 9 decodes Code B and pulling Pin 9 low puts the ICM7218 in a Shutdown mode.

NOTE 2 In the No Decode Mode, "Ones" represents "on" segments for all inputs except for the Decimal Point, where "Zero" represents "on" segments, (i.e. segments are positive true, decimal point is negative true).

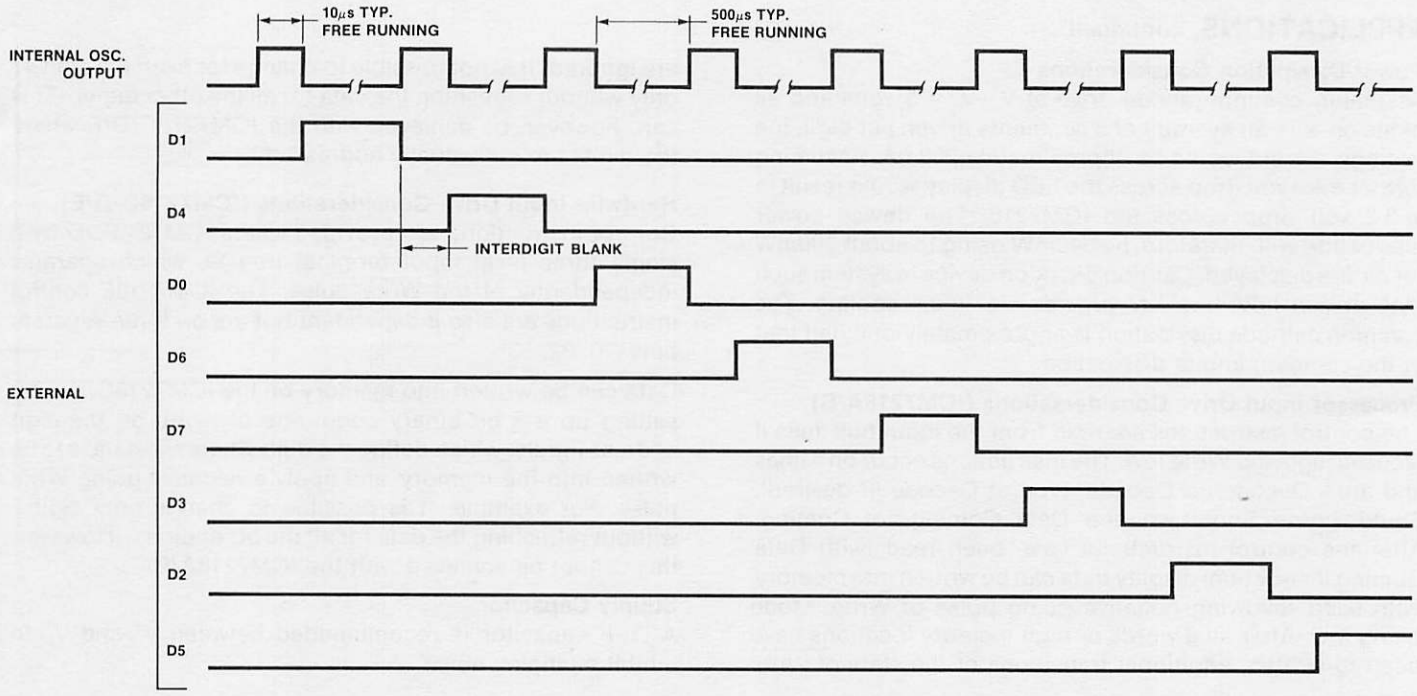


Figure 1: Multiplex Timing

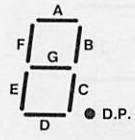


Figure 2: Segment Assignments

APPLICATIONS

Decode/No Decode

For the ICM7218A/B/E products, there are 3 input data formats possible; either direct segment and decimal point information-8 bits per digit or 2 BCD codes plus decimal point-5 bits per digit. The 7 segment decoder on chip may be disabled if direct segment information is inputted.

In the No Decode format, the inputs directly control the outputs as follows:

Input Data:	ID7 ID6 ID5 ID4 ID3 ID2 ID1 ID0
Output Segments:	$\overline{\text{D.P.}}$ a b c e g f d

The No Decode Mode, "Ones" represents on segments for all inputs except for the Decimal Point, where "zero" represents on segments.

Hexadecimal or Code B Decoding:
For all products, a choice of either Hexa or Code B decoding may be made. Hexa decoding provides 7 segment plus six alpha characters while Code B provides a negative sign (–), a blank (for leading zero blanking) and certain useful alpha characters for most numeric formats.

The four bit binary code is set up on inputs ID3-ID0.

Binary Code	0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
Hexa Code	0 1 2 3 4 5 6 7 8 9 A b C d E F
Code B	0 1 2 3 4 5 6 7 8 9 - E H L P (Blank)

$\overline{\text{Shutdown}}$

$\overline{\text{Shutdown}}$ performs several functions: it puts the device into a very low dissipation mode (typically 10μA at V^+-V^- = 5), turns off both the digit and segment drivers, stops the multiplex scan oscillator (this is the only way the scan oscillator can be disabled). However, it is still possible to input the memory during shutdown - only the output and read sections of the device are disabled.

Powerdown

In a Shutdown Mode, the supply voltage may be reduced to 2 volts without data being lost in memory. However, data should not be written into memory if the supply voltage is less than 4 volts.

Output Drive

The common anode output drive is approximately 200 mA per digit at a 12% duty cycle. With 5 segments being driven, this is equal to about 40mA per segment peak drive or 5mA average drive. The common cathode drive is approximately one half that of the common anode drive. If high impedance LED displays are used, the drive will be correspondingly less.

Inter Digit Blanking

A blanking time of approximately 10μs occurs between digit strobes to ensure that segment information is correct before the next digit drive thereby avoiding ghosting.

Leading Zero Blanking

This may be programmed into chip memory in the no-decode operation (each segment programmed for a zero for the blanked digits) or by using the 16th state (binary 15) with the Code B decoder.

Driving Larger Displays

If a higher average drive current per digit is required, it is possible to parallel connect digit drives together. For example, by paralleling pairs of digit drives together to drive a 4 digit display 10 mA average segment drive can be obtained.

APPLICATIONS, continued

Power Dissipation Considerations
Assuming common anode drive at $V^+-V^- = 5$ volts and all digits on with an average of 5 segments driven per digit, the average current would be approximately 200mA. Assuming further a 1.8 volt drop across the LED display would result in a 3.2 volt drop across the ICM7218. The device power dissipation will, therefore, be 640mW rising to about 900mW for all '8"s displayed. Caution: Position device in system such that air can flow freely to provide maximum cooling. The common cathode dissipation is approximately one half that of the common anode dissipation.

Processor Input Drive Considersations (ICM7218A/B)
The control instructions are read from the input bus lines if Mode is high and $\overline{\text{Write}}$ low. The instructions occur on 4 lines and are - Decode/no Decode, type of Decode (if desired), Shutdown/no Shutdown and Data Coming/not Coming. After the control instructions have been read (with Data Coming instruction) display data can be written into memory with each following negative going pulse of $\overline{\text{Write}}$, Mode being low. After all 8 words or digit memory locations have been re-written, additional transitions of the state of $\overline{\text{Write}}$ are ignored. It is not possible to change for example digit #7 only without refreshing the data for all the other digits. (This can, however, be achieved with the ICM7218C/D/E where the digits are individually addressed.)

Hardwire Input Drive Considerations (ICM7218C/D/E)
Control instructions are provided to the ICM7218C/D by a single three level input terminal (Pin 9), which operates independently of the $\overline{\text{Write}}$ pulse. The ICM7218E control instructions are also independent but are on three separate pins (10, 32, 33).

Data can be written into memory on the ICM7218C/D/E by setting up a 3 bit binary code (one of eight) on the digit address inputs, which define the digit where the data is to be written into the memory, and apply a negative going $\overline{\text{Write}}$ pulse. For example, it is possible to change only digit 7 without refreshing the data for all the other digits. (However, this cannot be achieved with the ICM7218A/B.

Supply Capacitor
A .1μF capacitor is recommended between V^+ and V^- to inhibit multiplex noise.

SWITCHING WAVEFORMS ICM7218

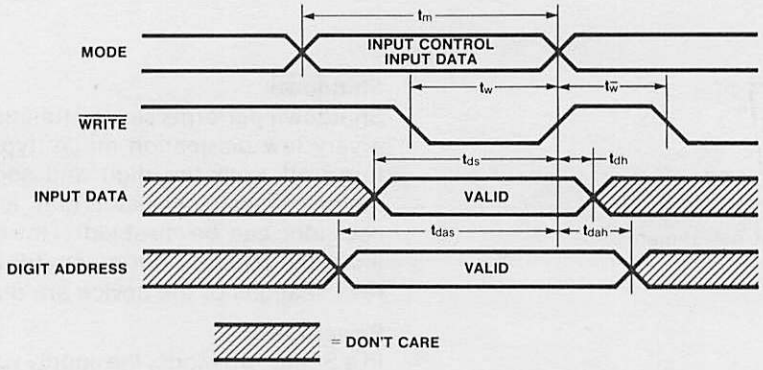


Figure 3

CHIP ADDRESS SEQUENCE ICM7218A and B

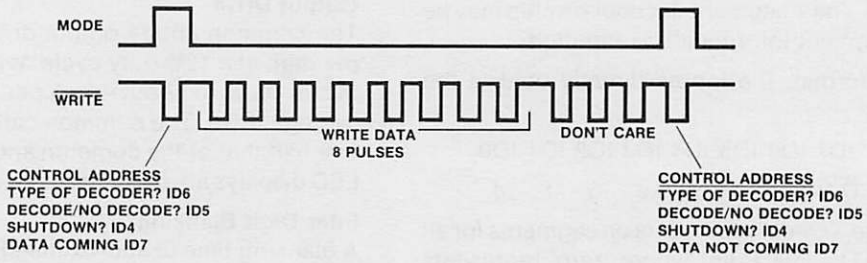


Figure 4

CHIP ADDRESS SEQUENCE EXAMPLE ICM7218C/D/E

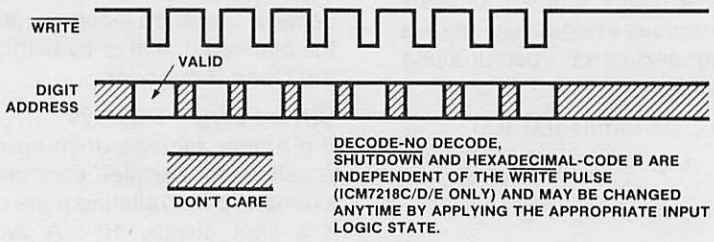
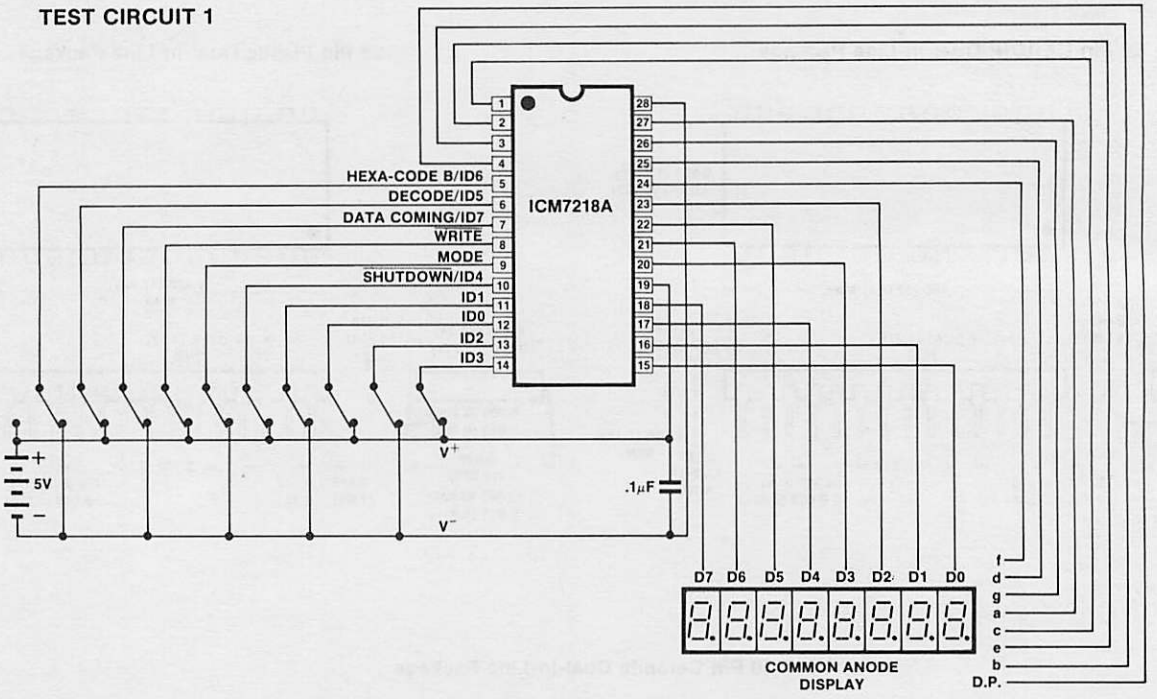


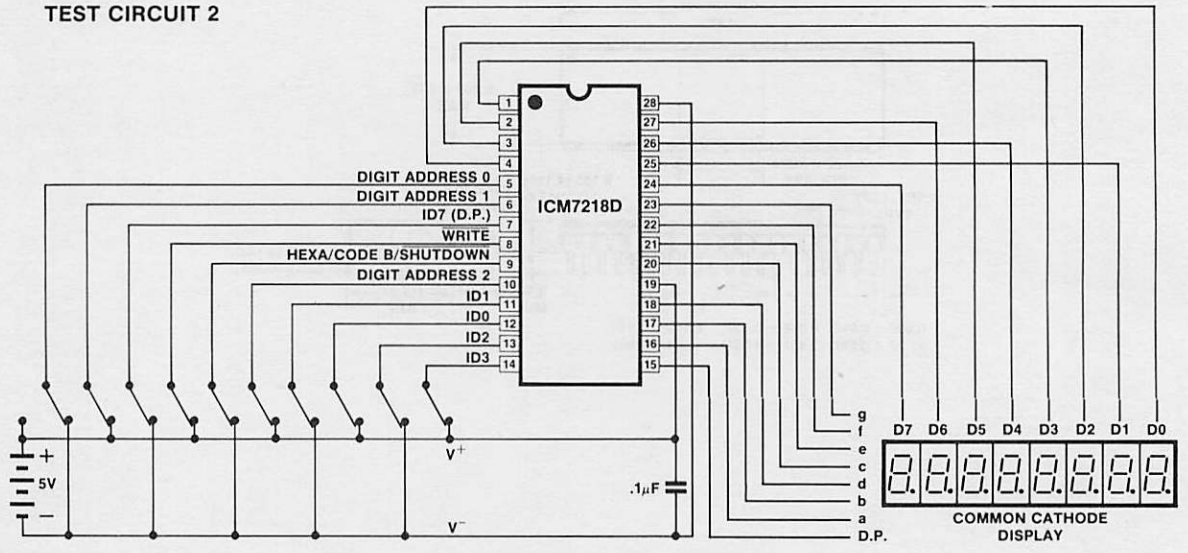
Figure 5

TEST CIRCUITS

TEST CIRCUIT 1

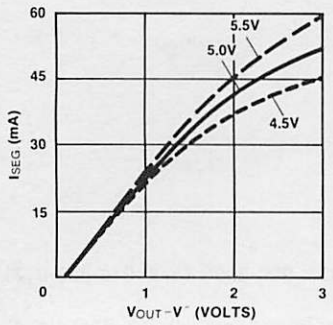


TEST CIRCUIT 2

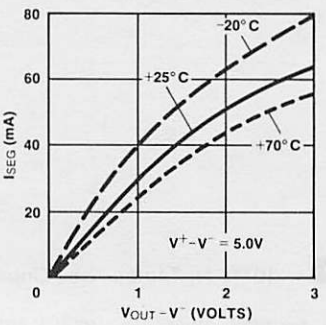


TYPICAL CHARACTERISTICS

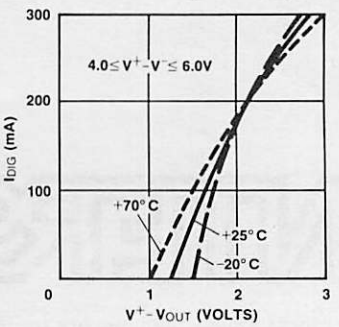
COMMON ANODE SEG. DRIVER
I_{SEG} VS. (V_{OUT}-V^-)
AT 25°C



COMMON ANODE SEG. DRIVER
I_{SEG} VS. (V_{OUT}-V^-)

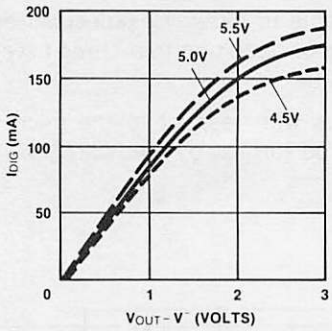


COMMON ANODE DIGIT DRIVER
I_{DIG} VS. (V^+-V_{OUT})

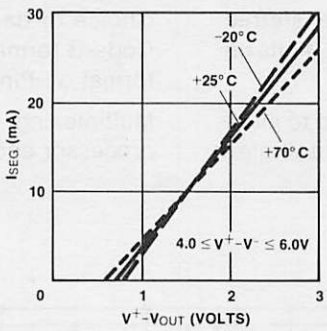


TYPICAL CHARACTERISTICS, continued

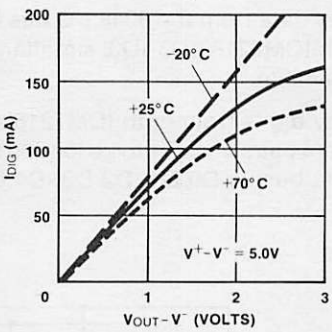
COMMON CATHODE DIGIT DRIVER I_{DIG} VS. (V_{OUT}-V^-) AT 25°C



COMMON CATHODE SEG. DRIVER I_{SEG} VS. (V^+-V_{OUT})



COMMON CATHODE DIGIT DRIVER I_{DIG} VS. (V_{OUT}-V^-)



APPLICATION EXAMPLES

8 DIGIT MICROPROCESSOR DISPLAY APPLICATION

The display interface (ICM 7218) is shown with an Intel 8048 microprocessor. The 8 bit data bus DB0/DB7 - ID0/ID7 transfers control and data information to the 7218 display interface on successive Write pulses. When Mode is high a control word is transferred. Mode low allows data transfer on a Write pulse. Eight memory address locations in the 8 x 8 static memory are automatically sequenced on each successive Write pulse. After eight Write pulses have occurred, further pulses are ignored and the display interface returns to normal display operation until a new control word is transferred. See Figure 4.

Decoding of the stored data in memory is defined by the control word and may be decoded in Hexadecimal, Code B, or No-Decode formats.

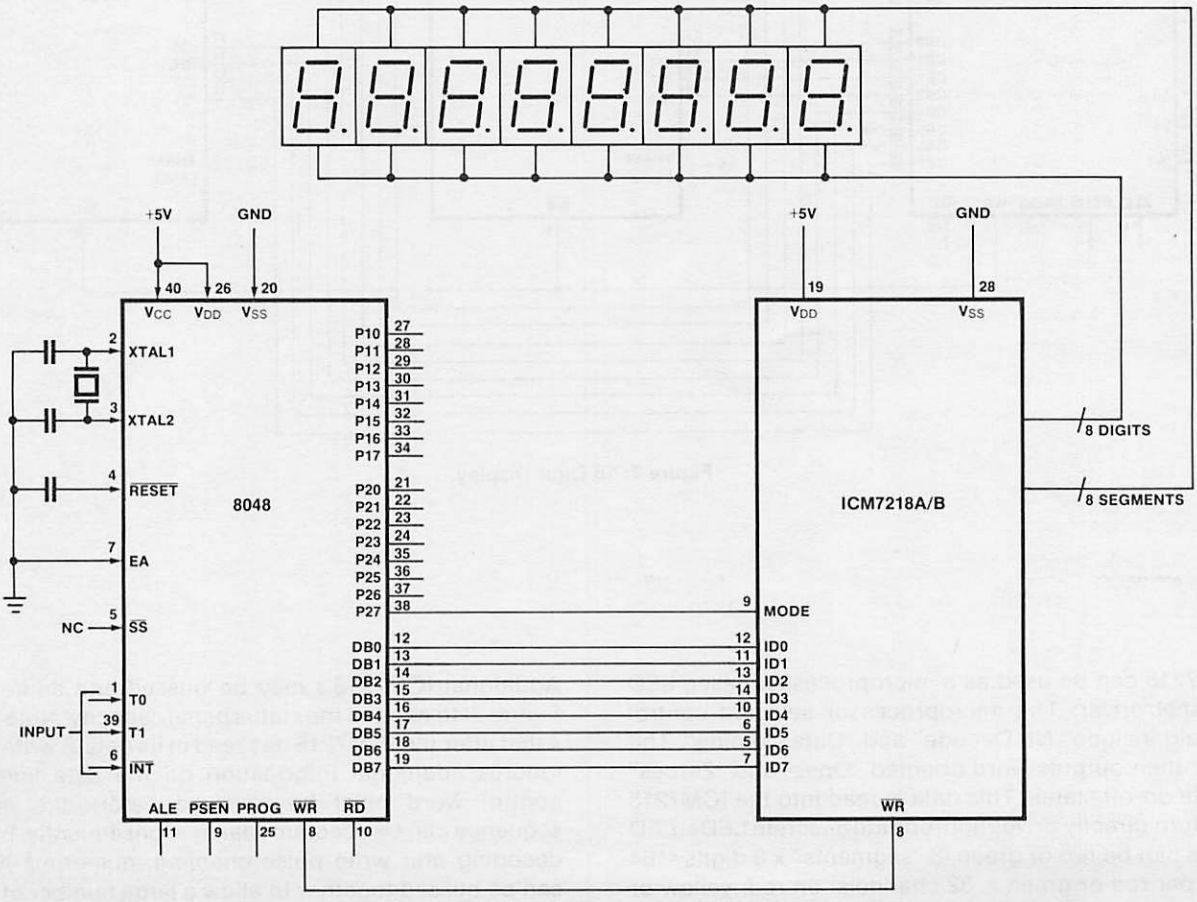


Figure 6: 8 Digit Microprocessor Display

16 DIGIT MICROPROCESSOR DISPLAY APPLICATION

Both ICM7218's are addressed simultaneously with a 3 bit word, DA2-DA0.

Display data from the 8048 I/O bus (DB7-DB0) is transferred to both ICM7218 (ID3-ID0) simultaneously, 4 bits + 4 bits on Write enable.

Display digits from both ICM7218's are interleaved to allow adjacent pairs of digits to be loaded sequentially on a single 8 bit data bus, ie D0 D1, D2 D3, D4 D5, etc..

Decimal point information (from 8048, P26 - P27) is supplied to the ICM7218 on bus lines ID7 to both devices.

Choice of decoding is available in either Hexadecimal or Code-B format by hardwiring or decoding to a Three Level format on Pin 9 of the ICM7218.

Multiplexing is asynchronous with respect to the microprocessor and is completely performed by the ICM7218.

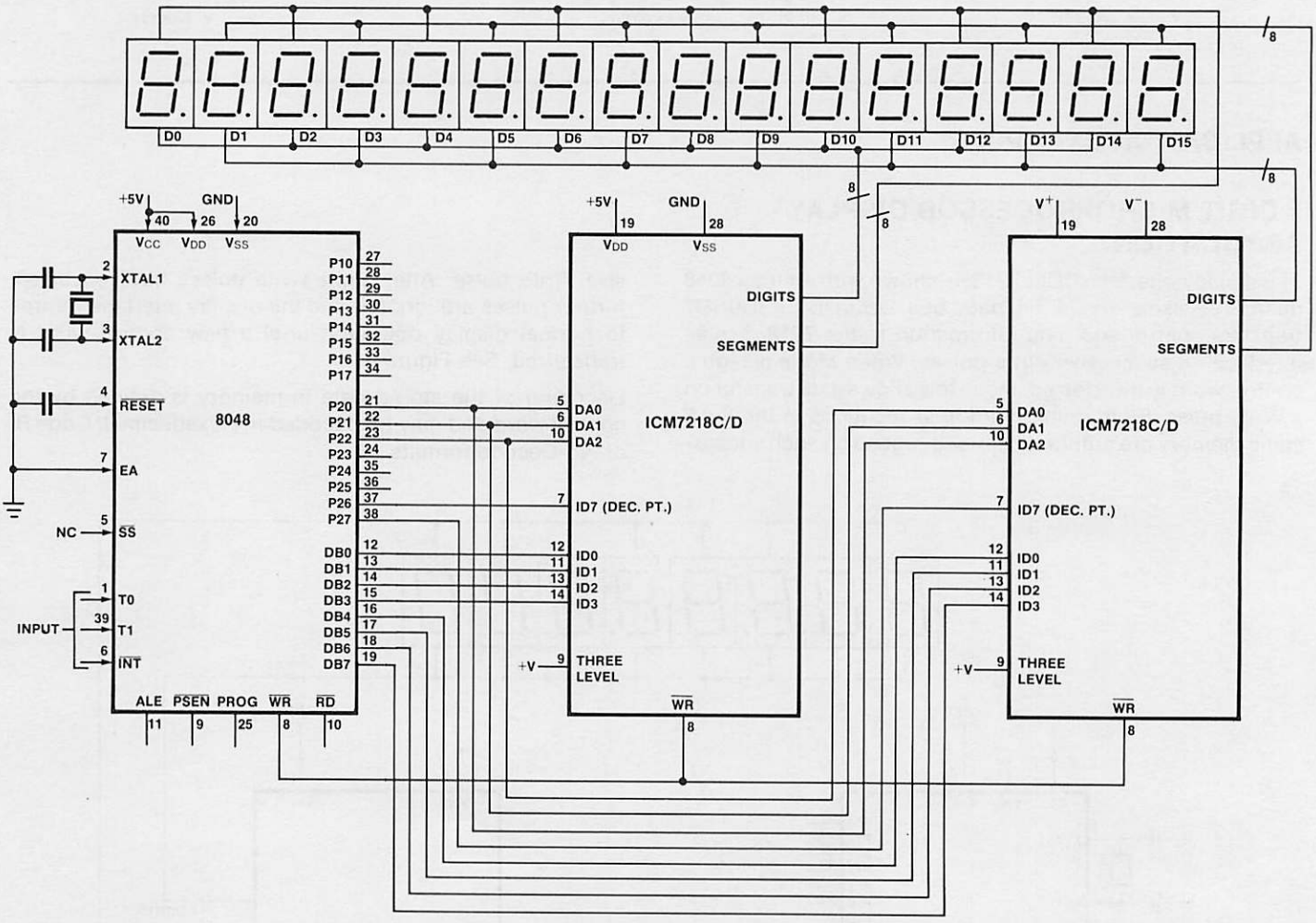


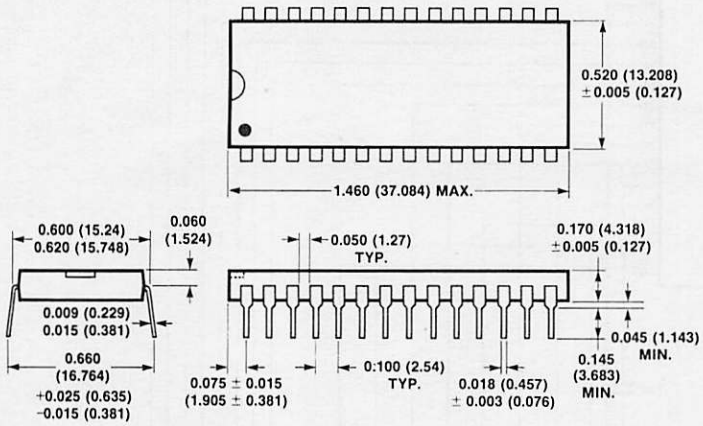
Figure 7: 16 Digit Display

The ICM7218 can be used as a microprocessor based LED status panel driver. The microprocessor selected control word would include "No Decode" and "Data Coming". The computer then outputs word oriented "Ones" and "Zeroes" to indicate on-off states. This data is read into the ICM7218 which in turn directly drives appropriate descrete LEDs. LED indicators can be red or green (8 "segments" x 8 digits = 64 dots ÷ 2 per red or green = 32 channels) on red, yellow or green (21 channels).

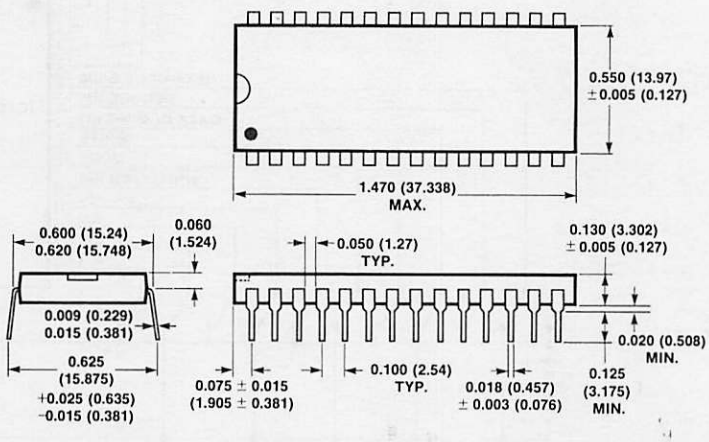
Additional ICM7218's may be bussed and addressed (see Figure 7) to expand the status panel capacity. Note per figure 4 that after the ICM7218 has read in its data (8 write pulses), it ignores additional information on the data lines. A new control word must be received before the next write sequence can be accommodated. Consequently, by address decoding and write pulse enabling, numerous ICM7218's can be bussed together to allow a large number of indicator channels.

PACKAGE DIMENSIONS

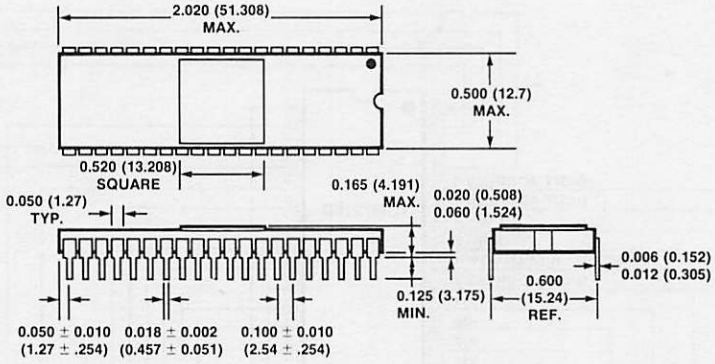
28 Pin CERDIP Dual-In-Line Package



28 Pin Plastic Dual-In-Line Package



40 Pin Ceramic Dual-In-Line Package



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