USC Viterbi School of Engineering

Department of Electrical Engineering - Systems

EE 459L - Embedded Systems Design Laboratory

The 74ACT715 Video Sync Generator

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Fall 2006

The 74ACT715 video sync generator is used to generate the necessary synchronization signals to produce a video signal. In most cases the composite sync from the sync generator is combined with a video signal from other circuitry to produce a composite video signal.

Initialization

When powered up the 74ACT715 is configured to run at rates compatible with RS-170 video but the internal clock in the chip must be enabled for it to start outputting sync signals. To enable the clock, bit 10 in the status register must be changed from a zero to a one. If no other registers in the chip have to be altered this can be done from a microcontroller by hardwiring the proper settings on the eight data input lines and then performing clear and load operations. The circuit show below (copied from Figures 6 in 74ACT715 datasheet) shows how this is done.

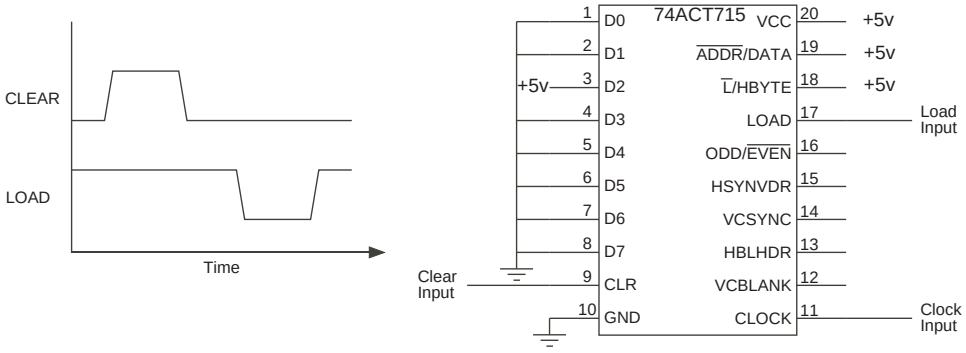


Figure 1: Initializing the 74ACT715 for RS-170 Video

This circuit requires two input signals (CLEAR and LOAD) in addition to the clock signal. The CLEAR line is pulsed from low to high to low to reset the device. After that the LOAD line is pulsed from high to low to high. The $\overline{\text{ADDR}}$/DATA line is in the high state to indicate that data is being loaded, and the $\overline{\text{L}}$/HBYTE is in the high state to cause the data to be loaded into the upper byte of the status register. With D2 of the data lines held high and the others low, this sets bit 10 in the status register to a one and enables the clock. Once these operations are done, the chip will start outputing RS-170 sync signals on the five output lines.

Output Signals

There are five output signals that come out of the 74ACT715 . Pin 16 is used to indicate whether the video is in the odd or even field of the frame. The other four are for various sync signals and internally the 74ACT715 generates ten different sync signals that can appear on these pins.

HBLANK	Horizontal blanking
VBLANK	Vertical blanking
CBLANK	Composite blanking (ANDing of HBLANK and VBLANK)
HSYNC	Horizontal sync
VSYNC	Vertical sync
CSYNC	Composite sync (ANDing of HSYNC and VSYNC)
HGATE	Horizontal gating (or horizontal drive)
VGATE	Vertical gating (or vertical drive)
CURSOR	Cursor position
VINT	Vertical interrupt

Since there are only four output pins for the sync signals only four of the above signals can actually be output at any one time. The states of bits 0, 1 and 2 in the status register determine which signals will appear on the four output pins. For the default settings the following four are output:

Pin Number	Pin Name	Signal Name	Signal Description
Pin 12	VCBLANK	CBLANK	Composite blanking
Pin 13	HBLHDR	HGATE	Horizontal gate (horzontal drive)
Pin 14	VCSYNC	CSYNC	Composite sync
Pin 15	HSYNVDR	VGATE	Vertical gate (vertical drive)

If a different set of sync signals is required, refer to the datasheet to see if bits 0, 1 and 2 in the status register can be set differently to get the desired signals on the four output lines.

Vertical Timing Signals

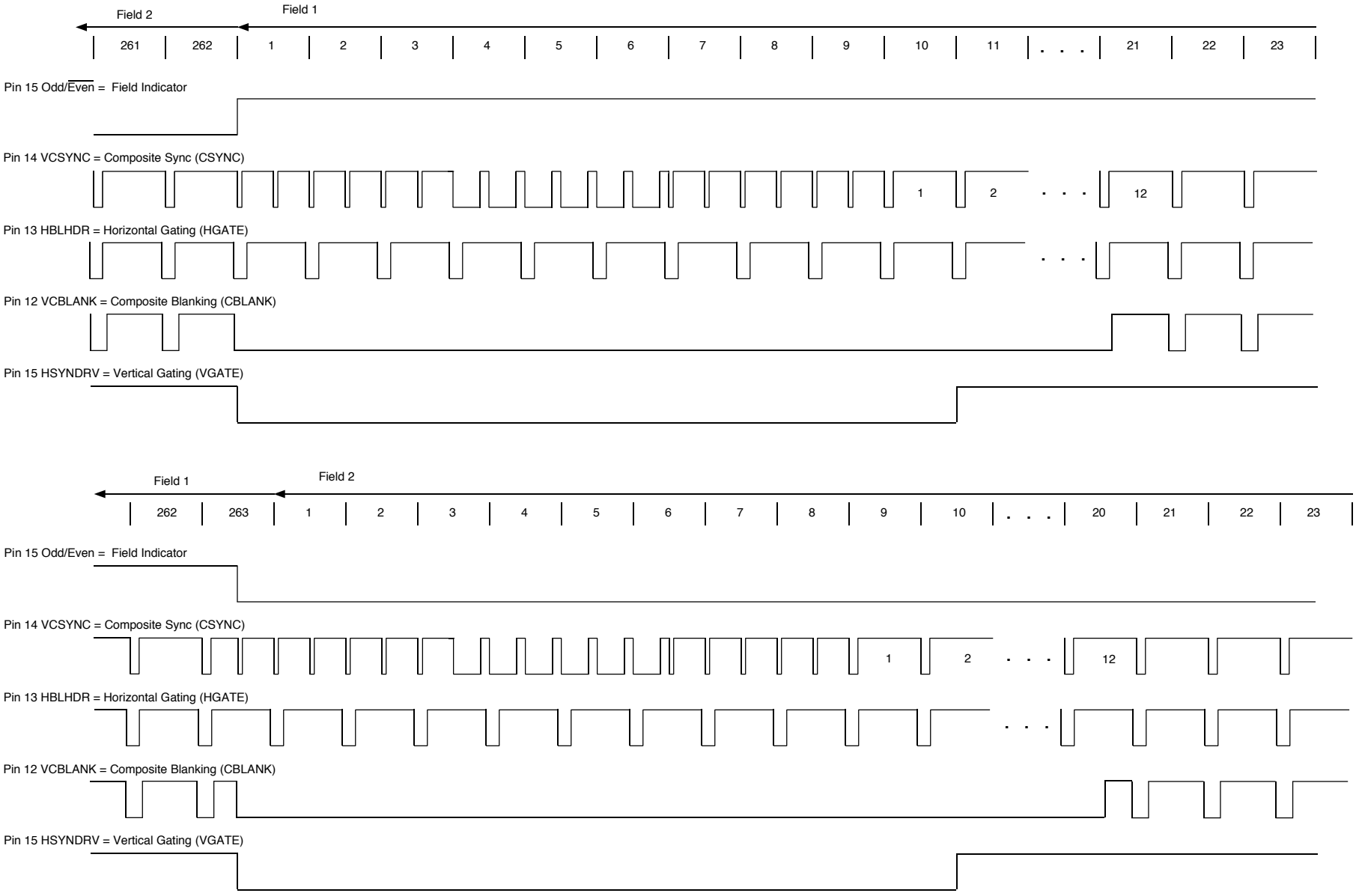
The diagrams on page 3 show the vertical time signals for both an odd and an even field. The vertical gating signal (VGATE) goes low at the beginning of vertical blanking and stays low for ten horizontal line times (635μsec). Vertical blanking stays low for twenty lines times (1271μsec). Note that the horizontal gating or horizontal drive signal (HGATE) is a consistent pulse train that give one equal length pulse for each horizontal line line. When counting vertical lines, this signal may work better than CSYNC since it does not have the serration and equalization pulses during the vertical blanking period.

Horizontal Timing Signals

The diagrams on page 4 show the horizontal timing signals. VCBLANK (composite blanking) is low for 10.9μsec during the blanking period of each horizontal line. The rest of the 63.5μsec line time is for active (viewable) video. The blanking period consists of a 1.5μsec front porch before the sync signal, a 4.7μsec sync period, and a 4.7μsec back porch after the sync signal. VCSYNC (composite sync) will be low during the sync period. The horizontal gating signal (HGATE) that appears on the HBLHDR output goes low at the start of the blanking period and returns high at the end of the sync period.

74ACT715 Timing Signals in RS-170 Mode

Vertical Timing Signals



Horizontal Timing Signals